

CLAIMS

We claim:

1 1. A system for synchronizing a plurality of data
2 channels, the system comprising:

3 a core circuit having a clock distribution circuit, the
4 core circuit providing a plurality of data streams at a
5 frequency of a core clock signal carried by the clock
6 distribution circuit;

7 a first phase-locked loop circuit generating a plurality of
8 clock signals, wherein a first clock signal from the plurality
9 of clock signals has the same frequency and substantially the
10 same phase as the core clock signal carried by the clock
11 distribution circuit; and

12 a plurality of channel circuits coupled to the core circuit
13 and to the first phase-locked loop circuit, the channel circuits
14 converting the plurality of data streams, received at a
15 frequency of the first clock signal, into a plurality of serial
16 data streams at a frequency of a second clock signal from the
17 plurality of clock signals.

1 2. The system of Claim 1, further comprising a second
2 phase-locked loop circuit coupled to the core circuit, the
3 second phase-locked loop circuit generating the core clock
4 signal and providing the core clock signal to the clock
5 distribution circuit.

1 3. The system of Claim 2, wherein the second phase-locked
2 loop circuit receives a sampled version of the core clock signal
3 from the clock distribution circuit to compensate for timing
4 differences associated with the clock distribution circuit.

1 4. The system of Claim 2, wherein the first phase-locked
2 loop circuit and the second phase-locked loop circuit receive a
3 reference signal through matched lines, which is used as a
4 frequency and phase reference.

1 5. The system of Claim 1, wherein a predefined phase
2 relationship exists among the plurality of clock signals and the
3 core clock signal carried by the clock distribution circuit.

1 6. The system of Claim 1, wherein the second clock signal
2 is distributed on a signal line having minimal skew to each of
3 the plurality of channel circuits.

1 7. The system of Claim 1, wherein at least one of the
2 plurality of clock signals is distributed to at least some of
3 the plurality of channel circuits via a register-to-register
4 transfer.

1 8. The system of Claim 7, wherein each register is
2 clocked by the second clock signal.

1 9. The system of Claim 1, wherein the first phase-locked
2 loop circuit is coupled to the core circuit, the first phase-
3 locked loop circuit providing the core clock signal to the clock
4 distribution circuit.

1 10. A method of synchronizing a plurality of data
2 channels, the method comprising:
3 receiving a reference clock signal;
4 generating a plurality of clock signals based on the
5 reference clock signal and providing a core clock signal from
6 the plurality of clock signals to a core circuit, wherein data
7 is transferred from the core circuit through a plurality of data
8 paths at a clock rate of the core clock signal;
9 receiving the data, transferred through the plurality of
10 data paths, by corresponding channel circuits at a clock rate of
11 a first clock signal from the plurality of clock signals, the
12 first clock signal having the same frequency and substantially
13 the same phase as the core clock signal; and
14 transforming the data received by each of the channel
15 circuits from a parallel to a serial data stream at a clock rate
16 of a second clock signal from the plurality of clock signals.

1 11. The method of Claim 10, wherein the plurality of clock
2 signals are generated with a predefined frequency and phase
3 relationship relative to each other and to the reference clock
4 signal.

1 12. The method of Claim 10, further comprising sampling a
2 version of the core clock signal within the core circuit and
3 adjusting a phase of the core clock signal to compensate for
4 timing variations within the core circuit.

1 13. The method of Claim 10, further comprising controlling
2 the distribution of the second clock signal to each of the
3 channel circuits to minimize skew.

1 14. The method of Claim 10, further comprising
2 distributing at least one of the plurality of clock signals to
3 each of the channel circuits by a register-to-register transfer.

1 15. The method of Claim 14, wherein each of the registers
2 is clocked by the second clock signal.

16. A system comprising:

a first phase-locked loop circuit generating a plurality of clock signals, including a first clock signal; and

a plurality of channel circuits, coupled to the first phase-locked loop circuit, that each receive a data stream from a core circuit at a frequency of a core clock signal which has the same frequency and substantially the same phase as the first clock signal, wherein at least one of the plurality of clock signals is distributed to at least some of the plurality of channel circuits via a register-to-register transfer.

17. The system of Claim 16, wherein the register-to-register transfer occurs at a frequency of a second clock signal from the plurality of clock signals.